WHAT IS CLAIMED IS:

1. A MOS transistor comprising:

a semiconductor substrate having a trench formed therein, wherein the trench has a predetermined width forming an active region;

a channel region made from silicon, wherein the channel region has a predetermined width and a predetermined thickness on a bottom of the trench;

a gate oxide film is located on the channel region;

a source and drain region buried in the interior of the trench;

a gate groove having a predetermined width is located on the gate oxide film in the interior of the trench; and

a gate electrode buried in the gate groove.

2. The MOS transistor of claim 1, wherein the source and drain region includes a polycrystalline material doped with impurities.

3. The MOS transistor of claim 1, wherein the source and drain region includes a SiGe film.

4. The MOS transistor of claim 3, wherein the SiGe film has a ratio of Si to Ge in a range of 9 : 1 to 7 : 3.

5. The MOS transistor of claim 4, wherein the SiGe film is a polycrystalline material doped with impurities.

6. The MOS transistor of claim 1, wherein the channel region has a thickness of 1000 – 3000Å.

7. The MOS transistor of claim 1, further comprising:

an insulation film is located on a top surface of the source and drain region; and

side walls made from a nitride film located on sides of the gate groove.

8. The MOS transistor of claim 7, wherein the insulation film is a tetra ethyl ortho silicate film.

9. A method of fabricating a MOS transistor, comprising:

forming a trench by selectively etching a semiconductor substrate;

forming a channel region having a silicon layer with a predetermined width in a bottom of the trench;

forming a gate oxide film on the channel region;

forming a source and drain film on the gate oxide film and within the trench, wherein the source and drain film buries the trench;

forming a gate groove with a predetermined width to expose at least a portion of the gate oxide film by selectively etching the source and drain film; and

forming a gate electrode by forming a silicon layer on the exposed gate oxide film such that the gate groove is buried.

10. The method of claim 9, after the silicon layer is formed on an overall top surface of the semiconductor substrate including the trench and the gate oxide film is formed on the silicon layer, the channel region and the gate oxide film are sized to a predetermined width, by forming a pattern of a photosensitive film covering the predetermined width of the gate oxide film within the trench on the gate oxide film and etching the exposed gate oxide film and the silicon layer using the pattern of the photosensitive film as a mask.

11. The method of claim 9, wherein the silicon layer has a thickness between 1000 - 3000Å.

12. The method of claim 9, wherein the gate oxide film has a thickness between 100 - 500Å.

13. The method of claim 9, wherein the source and drain film is formed from a SiGe film.

14. The method of claim 13, wherein the SiGe film is formed by depositing a polycrystalline SiGe film doped with the impurities.

15. The method of claim 14, when the SiGe film is formed, impurities are doped at the same time of depositing the SiGe film.

16. The method of claim 14, wherein the SiGe film is deposited to have a ratio of Si to Ge in a range of 9 : 1 to 7 : 3.

17. The method of claim 13, further comprising:

performing a thermal process on the SiGe film after the SiGe film is deposited.

18. The method of claim 9, wherein the source and drain film is formed by depositing the source and drain film on an overall top surface of the semiconductor substrate including the interior of the trench, and subsequently removing a portion of the source and drain film such that the source and drain film remains only in the interior of the trench.

19. The method of claim 18, further comprising:

forming a tetra ethyl ortho silicate film on the overall top surface of the semiconductor substrate including the source and drain film; and

planarizing the tetra ethyl ortho silicate film until the semiconductor substrate is exposed.

20. The method of claim 19, wherein the planarization of the tetra ethyl ortho silicate film is performed by one of an etch-back processing and a chemical mechanical polishing.

21. The method of claim 19, further comprising:

forming side walls on both sides of the gate groove.

22. The method of claim 21, wherein the side walls are formed form a nitride film.